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EXAMINER	
LUU, MATTHEW	
ART UNIT	**PAPER NUMBER**
3663	

DATE MAILED: 03/02/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/620,150	GONZALEZ ET AL.	
	Examiner	Art Unit	
	LUU MATTHEW	3663	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 December 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-32,65-67 and 72-76* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-32,65-67 and 72-76* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 December 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. Claims 1-32 and 76 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claim 1, lines 5 and 6, "said output signals" has no antecedent basis.

Regarding claim 8, line 2, "said modifications to said multiple, modified graphics command streams" has no antecedent basis.

Regarding claim 11, line 2, "said portions of said graphics screen" has no antecedent basis.

Regarding claim 14, line 2, "said portions of said graphics screen" has no antecedent basis.

Claim 76 is depending on a canceled claim 71.

Dependent claims are considered rejected for incorporating the defects from their respective parent claims by dependency.

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 1-32 and 65-67 and 72-76 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Regarding independent claims 1, 65, 66 and 67, the specification fails to provide a clear meaning of the claimed "a graphics command replicator". Therefore, for the purpose of examining, "a graphics command replicator" is interpreted as " a graphics command generator".

Furthermore, it is unclear what exactly is the "load balancing ratio". How exactly is the load balancing ratio can be assigned to each of the plurality of video cards? What exactly is the circuitry that assigns the load balancing ratio to each of the plurality of video cards?

Dependent claims are also considered rejected for incorporating the defects from their respective parent claims by dependency.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claim 1 is, ***as best understood***, rejected under 35 U.S.C. 103(a) as being unpatentable over Taylor (WO 97/14133) in view of Callway (EP 1061434) and Ebihara (US 2002/0130870).

Regarding claim 1, Taylor discloses (Fig. 1) an accelerated graphics processing subsystem comprising:

a graphics command generator (host computer system 101);

a plurality of video cards (subsystems 103, which includes the VGA 104) (Page 6, line 8); and

a video merger hub (DAC/LUT 109, see also Figs. 2A and 2B).

Taylor fails to teach a mechanism to synchronize the plurality of video cards signals and the load balancing ratio assigned to each of the plurality of video cards.

However, Callway discloses (Figs. 1 and 3) a mechanism (controller 130) for synchronizing (synch control) a plurality of video cards signals.

Therefore, it would have been obvious to a person of ordinary skill in the art to use the synchronization circuit of Callway into the graphics processing systems of Taylor to synchronize the plurality of video signals which allows these signals to be displayed simultaneously on the display screen.

As to the new added limitations, the vertical refresh rate of the output signals is the well-known vertical SYNC signal as disclosed by Callway (Column 5, line 46-49). Furthermore, it is well known in the art that every window display on the display screen would have the vertical resolution as well as the horizontal resolution that define the dimension of the window on the display screen.

As to the load balancing ratio, as best understood, Ebihara (US 2002/0130870) discloses (Figs. 5 and 6) a graphics subsystem block (GSB 100), which includes a plurality of four subsystem modules (GSMs 4), wherein each GSM (4) is assigned with different load percentage (Sections 3, 82, 88 and 91).

Therefore, it would have been obvious to the person of ordinary skill in the art to use the load balancing system of Ebihara into the graphics processing systems of Taylor to balance the execution load among the video cards of Taylor.

Claim Rejections - 35 USC § 103

6. Claims 2-32 and 65-67 and 72-76, ***as best understood***, are rejected under 35 U.S.C. 103(a) as being unpatentable over Taylor in view of Callway and Ebihara as applied to claim1 above, and further in view of Lefebvre (The Hewlett-Packard Journal, May 1998).

Regarding claim 2, Taylor discloses (Fig. 1) the number of graphics command streams (2 pixel data streams) is equal to the number of the plurality of video cards (2 subsystems 103).

Taylor fails to teach the graphics command is a software module.

However, Lefebvre teaches that "OpenGL is a specification for a software-to-hardware application programming interface, or API, that defines operations needed to produce interactive 3D applications. It is designed to be used on a wide range of graphics devices, including simple frame buffers and hardware-accelerated geometry processor systems. Lefebvre further teaches "OpenGL is targeted for use on a range of new graphics devices for both UNIX based and Windows NO-based operating system platforms. These systems differ in both capabilities and performance."

Therefore, it would have been obvious to the person of ordinary skill in the art to use the OpenGL software into the graphics processing system of Taylor to generate a software-to-hardware application programming interface since this is well known in the art.

Regarding claim 3, Taylor discloses (Figs. 2A and 2B) each portion of the screen (110) displays a graphics command stream.

Regarding claim 4, Taylor discloses (Fig. 1) the plurality of video cards (103) is combined into a signal graphics output signal (DAC/LUT 109).

Regarding claim 5, Taylor discloses (Fig. 1) the display (110) is an LCD (Page 6, line 8).

Regarding claim 6, Lefebvre teaches that "OpenGL is a specification for a software-to-hardware application programming interface, or API, that defines operations needed to produce interactive 3D applications.

Regarding claim 7, Lefebvre further teaches "OpenGL is targeted for use on a range of new graphics devices for both UNIX based and Windows NO-based operating system platforms. These systems differ in both capabilities and performance."

Regarding claims 8-10, the clipping command in a 2D and 3D graphics processing system is conventional in the art.

Regarding claims 11-16, Taylor discloses (Fig. 2A) the sum of all the portions of the graphics screen combine to generate a full graphics screen. And Fig. 2B shows the overlapping regions. Furthermore, the non-overlapping graphics windows are well known in the art.

Regarding claims 17-19, it is well known in the art that a video board might include with more than one graphic processing units (GPUs).

Regarding claims 20-22, Callway discloses (Fig. 3) the synch control circuit includes a phase lock loop (PLL 352) and a voltage control oscillator (VCO 353).

Regarding claim 23, Taylor discloses (Fig. 1) a video merger hub (DAC/LUT 109, see also Figs. 2A and 2B).

Taylor fails to discloses a video switch controller.

However, Callway discloses (Fig. 1) a video switch (141 or 143); a video switch controller (controller 130); a microcontroller (130); and a video output (RGB OUT 1). It would have been obvious to the person of ordinary skill in the art to use the video switch controller (130) of Callway into the video merger hub of Taylor to provide alternating frames of video data to the video merger hub.

Regarding claims 24-26 and 67, and 72-76, Callway further discloses (Fig. 1) the video ports (151 and 152) combine the output signals from a plurality of video cards (110 and 120) into a single graphic output and sequentially display the signal on a display device by triggering routing switches at appropriate time intervals (Section 0021).

Regarding claims 27-32, as best understood, Ebihara (US 2002/0130870) discloses (Figs. 5 and 6) a graphics subsystem block (GSB 100), which includes a plurality of four subsystem modules (GSMs 4), wherein each GSM (4) is assigned with different load percentage (Sections 3, 82, 88 and 91).

Therefore, it would have been obvious to the person of ordinary skill in the art to use the load balancing system of Ebihara into the graphics processing systems of Taylor to balance the execution load among the video cards of Taylor.

Regarding claims 65-66, these claims are the combination of claims 1 and 23-26. Thus, see the rejections as set forth above.

Response to Arguments

7. Applicant's arguments with respect to claims 1-32, 65-67 and 72-76 have been considered but are moot in view of the new ground(s) of rejection.

Applicant argues, at page 12, the last paragraph, with respect to the Graphics Command Replicator (GCR), by pointing to paragraph 39 in the specification.

However, there is no where in this paragraph 39 that describes the graphics command being replicated, i.e., there is no replication being discussed.

Applicant argues, at page12 and 13, that the terms "Genlock", "master timing devices', "slaves of said master timing regulating device", and "load balancing ratio" are all well known in the filed of computer science. The examiner respectfully disagrees.

Since all of these well known features, i.e., "Genlock", "master timing devices', "slaves of said master timing regulating device", and "load balancing ratio" being claimed in the invention, it is unclear what exactly does the Applicant invent beside theses known features.

Applicant further argues, at page 14, by asserting that the "Load Balancing" is well known to be used in a network/server system. However, the claimed invention has nothing to do with the network/server system. This "Load Balancing" feature may be well known in the network/server system, but it may not be well-known in the plurality of video cards system.

Regarding to claims 1-32, 65-67 and 72-76, note the new ground of rejections under 112 paragraphs and the prior art rejections as set forth above.

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to LUU MATTHEW whose telephone number is (571) 272-7663. The examiner can normally be reached on Flexible Schedule.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, JACK KEITH can be reached on (571) 272-7663. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

M. Luu

MATTHEW LUU
PRIMARY EXAMINER